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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No.

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
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Additional inventors are being named on the _____ *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

OPERATING FREQUENCY REDUCTION FOR TRANSVERSAL FIR FILTER

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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ENCLOSED APPLICATION PARTS ***(check all that apply)***

☒ Specification *Number of Pages* 7 ☐ CD(s), Number _____

☒ Drawing(s) *Number of Sheets* 10 ☐ Other (specify) _____

☐ Application Date Sheet. See 37 CFR 1.76

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☒ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

☒ The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 501456

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE Amount ($): $80.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

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TELEPHONE 1-613-788-2242

Date August 28, 2003

REGISTRATION NO. 22,243 *(if appropriate)*

Docket Number: 102003-4

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

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OPERATING FREQUENCY REDUCTION FOR TRANSVERSAL FIR FILTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to allowing double-edge clocking and reducing frequency of operation in high-speed analog circuitry. More particularly, the present invention relates to a method and a system for allowing double-edge clocking to reduce the frequency of operation of a transversal FIR filter whose general functionality can be used to implement a Feed Forward Equalizer (FFE) and a Decision Feedback Equalizer (DFE).

2. Description of Related Art

A standard transversal FIR filter includes serial transmitter block includes a set of delay elements, a set of respective multiplication elements, and a summing node.

The delay elements of the transversal filter all operate using the same clock, referred to as the High Speed Clock, which has a period T which is equal to the Unit Interval (UI) of the serial data stream. In practical applications, the delay element is implemented using a Flip-Flop that samples data present on an input on a given clock edge, and holds the data value on an output for the duration of a clock period.

In certain cases, it is advantageous to reduce the operating frequency of the clock signal for reasons of technical feasibility or power consumption optimization. It is possible to split the delay elements in the transversal filter into two groups, one of which latches data on the rising edge of the clock signal, the other latching data on the falling edge of the clock signal. This will allow a High Speed clock signal with a period T which is effectively twice the duration of a UI, it also implies that the data sample is held by the delay element for two UI.

In order to improve Bit Error Rate performance in communications systems, a transversal FIR filter is sometimes used in the receiver or the transmitter to correct for InterSymbol Interference (ISI). An FFE is commonly used in a transmitter, while a receiver will generally contain a DFE.

An FFE is an extension of a standard serializer transmit block, where data bits are shifted through delay elements to be transmitted one at a time, but with a partial contribution from other bits contained in the delay structure. An FFE serial transmitter includes a set of delay elements, a set of multipliers, and a summing node. The delay elements all operate using the same High Speed clock signal, and shift data forward on only one edge (usually rising) of the clock. An FFE requires that the output of a delay element be held for no more than one UI. Thus, the period T of the High Speed clock is generally equal to one UI for proper functionality.

A DFE receiver block is an extension of a standard serial bit receiver block. A DFE receiver block includes a slicer, a set of delay elements, a set of multipliers, and a summing node. The slicer and delay elements all operate using the same High Speed clock signal, and sample data on only one edge (usually rising) of the clock. A DFE requires that the data sample be held at the output of a delay element for not more than one UI. Thus, in order for a DFE receiver block to function correctly, the period T of the High Speed clock signal must be equal to the Unit Interval of the incoming data stream.

In both the case of the FFE and DFE, increasing the High Speed clock period by a factor of two would cause a functional failure. Therefore, there is a need to have an efficient method and system that will allow a DFE to function using a double edge clocking scheme, so that the frequency of operation of the transversal filter in an FFE or DFE can be reduced.

SUMMARY OF INVENTION

The present invention provides a method and a system for using a double-edge clocking scheme and reducing the frequency of operation for a transversal FIR filter. The transversal filter consists of all analog sections. All analog sections operate in accordance with a clock signal that has a period, which is two times longer in duration than the serial data Unit Interval.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 a simplified block diagram of a serial bit stream receiver;

FIG. 2 a simplified block diagram of a deserializer circuit that implements a double edge clocking scheme;

FIG. 3 a simplified block diagram of a receiver that implements a DFE;

FIG. 4 a simplified block diagram of a 2:1 Multiplexer;

FIG. 5 a block diagram of the embodiment of the serial bit stream receiver constructed according to the present invention;

FIG. 6 a block diagram of the exemplary implementation of the combination Multiplexer/Multiplier (MUX/MUL);

FIG. 7 a simplified block diagram of a serial bit stream transmitter;

FIG. 8 a simplified block diagram of a transversal FIR filter;

FIG. 9 a block diagram of the embodiment of the serial bit stream transmitter constructed according to the present invention;

FIG. 10 a block diagram of serial transmitter with FFE.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and a system for allowing the use of double-edge clocking to reduce the frequency of operation of a transversal FIR filter structure.

The invention comprises of a set of 2:1 multiplexers used in combination with a set of multiplier sub-blocks contained in a transversal FIR filter.

In order to appreciate the advantages of the present invention, it will be beneficial to describe the invention in the context of an exemplary 10Gb/s Serializer/Deserializer (SerDes) receiver block.

FIG. 8 represents a general transversal FIR filter, where the data present at **800** is shifted forward every time T, which is represented by the delay elements **810** , where the shifted and delayed data is represented by **802.** As the data passes through the filter, data present at **800** and **802** is multiplied by a respective factor at **804.** All of the products are summed up at **806,** to generate the output of the filter **808.** A transversal FIR filter requires that the data sample be held at the output of a delay element for not more than T.

In **FIG. 7** a transmitter is represented as a standard serial bit stream shifter, where the data present at **708** is shifted toward the output **704** through the delay elements **706.** The High Speed clock at **700** has a period T that is equal to the data UI, where for a 10Gb/s application, is represented by the value 100ps.

FIG. 10 represents a transmitter with Feed Forward Equalization capability. Serial data is presented at **1000** and is shifted through delay elements **1004,** on the rising edge of clock **1002,** which has a specific period T. The bits are held at the output of delay elements **1014** for duration equal to clock period T, and the bit value is multiplied by the co-efficient factor **1008,** by multiplier **1006.** The multiplier outputs **1016** are all summed at **1010** to generate the transmitter output **1012.**

In **FIG.1** a receiver is represented as a standard serial bit stream receiver, where the data present at **100** has a UI of 100ps for a data rate of 10Gb/s. The High Speed Clock at **102** has a period T that is equal to the data UI, where for a 10Gb/s application, is represented by the value 100ps. The slicer **104** and delay elements **106** are active on the rising edge of the high speed clock. The depth of the serial FIFO, or number of delay elements is determined by the particular application.

In **FIG. 2** the receiver FIFO is modified to accommodate a high speed clock **112** that has a period T that is equal to two times the data UI at **110.** This means that both edges of the clock are used to latch incoming data, so there needs to be two classes of slicer and delay elements. Slicer **114** and delay elements **118** are active on the rising edge of the clock, while slicer **116** and delay elements **120** are active on the falling edge of the clock. The overall functionality of this receiver is equivalent to that described in **FIG. 1,** except that the receive clock frequency **112** is half that of **102.**

The receiver in **FIG. 3** represents a standard Decision Feedback Equalizer scheme, where the serial data input **200** is combined with contributions from past bit decisions made by slicer **210,** and which are held for one UI by delay elements **214.** The data bits **216** held by the delay elements are multiplied by respective co-efficient factors **212,** and all the products **218** are summed together at summing node **208.** The summing node value is fed back to the data path and subtracted from the incoming data stream at **204** to produce the composite equalized slicer input **206.** In this scheme, the high speed clock **202** has a period T that is equal to one UI.

In the present embodiment of the current invention, a 2:1 multiplexer **408,** as described in **FIG. 4** , having two inputs **400** and **402,** and one output **406,** the value of such an output being determined by the polarity of the selector **404,** is used to reduce the high speed clock frequency of a transversal FIR filter without affecting the intended theoretical functionality.

In **FIG. 9,** a transmitter using the current invention is described. There are two sets of delay elements which are introduced. Delay elements **906** are active on the rising edge of high speed clock **900** and delay elements **908** are active on the falling edge of the high speed clock, and will clock in data from **904** and **902** respectively. Since both

edges of the clock are used, the clock period T of **900** can be increased to 2 times the data UI at **930.** This means that all delay elements will hold their corresponding data bit **932** or **934** for two UI. The 2:1 multiplexer **916** is then used to correct this problem, by using the high speed clock as a select input at **914,** it will feed the corresponding multiplier **922** with the correct data bit **932** or **934,** depending on the clock polarity, for the appropriate time of only one UI. The products **924** are summed at **926,** the result of which will be the transmitter output **930.**

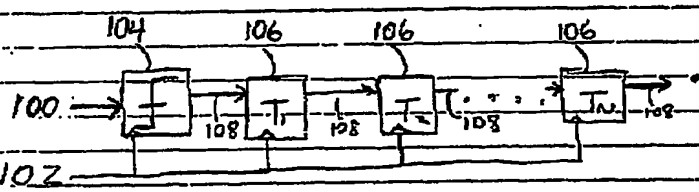
In **FIG. 5,** a receiver using the current invention is described. There are two sets of slicers and delay elements which are introduced. Slicer **508** and delay elements **520** are active on the rising edge of high speed clock **502** and slicer **509** and delay elements **522** are active on the falling edge of the high speed clock. Since both edges of the clock are used, the clock period T of **502** can be increased to 2 times the data UI at **500.** This means that all slicers and delay elements will hold their corresponding data bit **518** or **526** for two UI. The 2:1 multiplexer **516** is then used to correct this problem, by using the high speed clock as a select input at **524,** which will feed the corresponding multiplier **514** with the correct data bit **518** or **526,** for the appropriate time of only one UI. The products **528** are summed at **510** and fed back at **504** to produce the equalized slicer input **506.**

In **FIG. 6,** sub-blocks **516 and 514,** including all related inputs and outputs, are combined to define a Multiplexer/Multiplier (MUX/MUL) **614,** which has co-efficient input **600,** data select input **602,** input data zero **606,** and input data one **604,** as inputs, and output product **608.** Combining the multiplexer and multiplier into a single block will further optimize power consumption in the circuit, as well as related silicon area.

ABSTRACT

A method for allowing double-edge clocking and to reduce the frequency of operation for a transversal Finite Impulse Response (FIR) filter. The transversal FIR filter consists of analog sections. All analog sections operate in accordance with a clock.

FIG. 1



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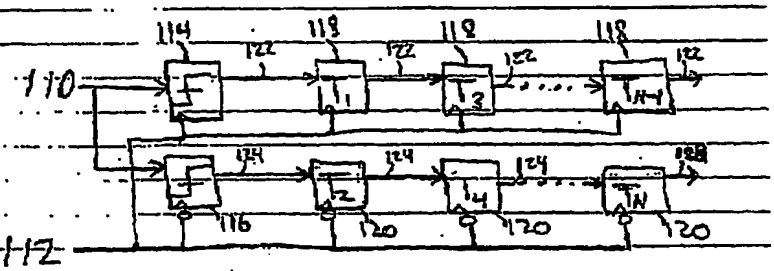
Operating Frequency Reduction for Transversal F.I.R. FILTERS

FIG. 2



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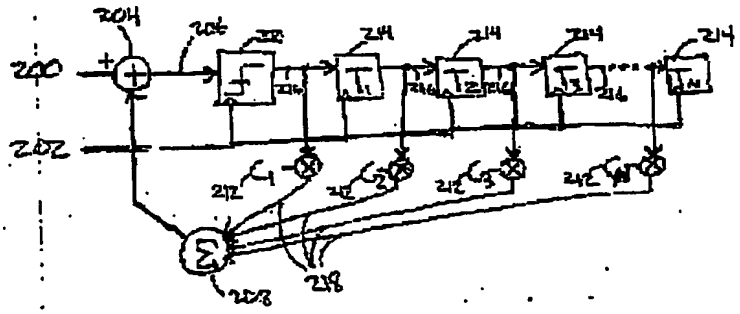
- Operating Frequency Reduction for Transversal FIR Filters

FIG. 3



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Operating Frequency Reduction for Transversal FIR Filter.

FIG. 4

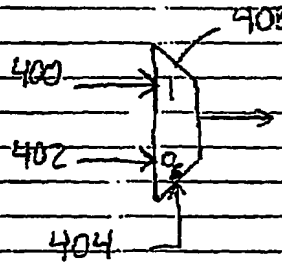

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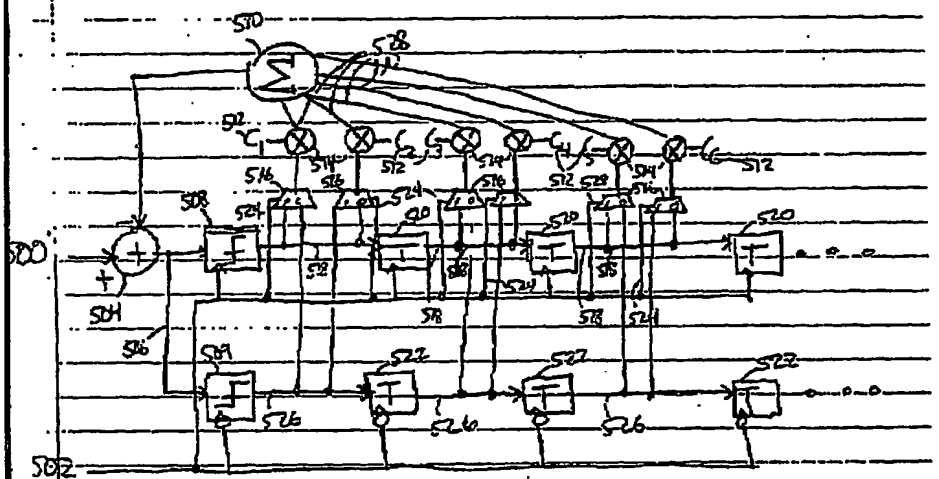
FIG. 5



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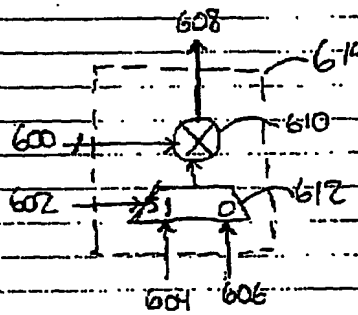
Operating Frequency Reduction for Transversal FIR Filters

FIG. 6



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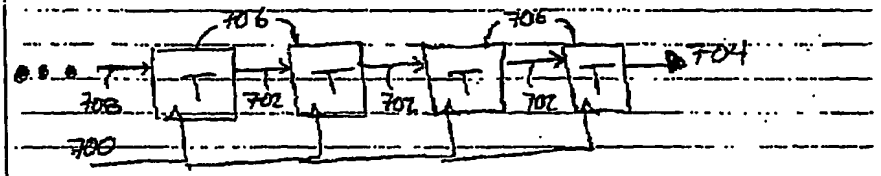
Operating Frequency Reduction for Transversal FIR Filter

FIG. 7



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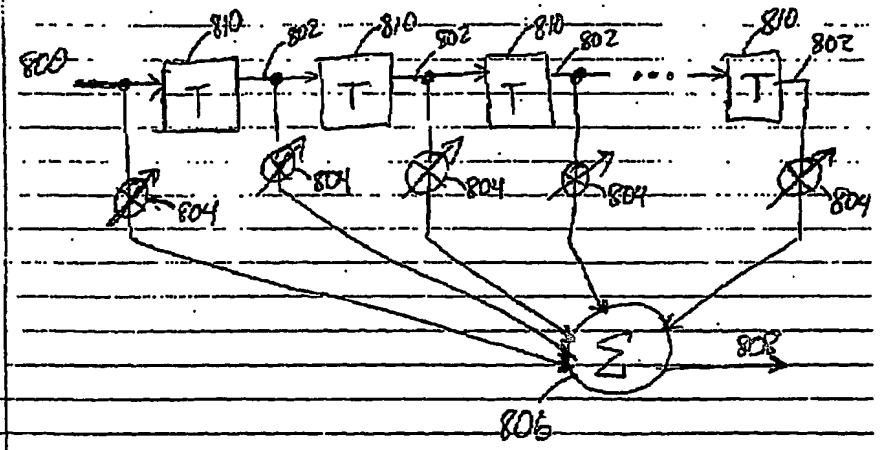
Operating Frequency Reduction for Transversal FIR Filter.

FIG. 8



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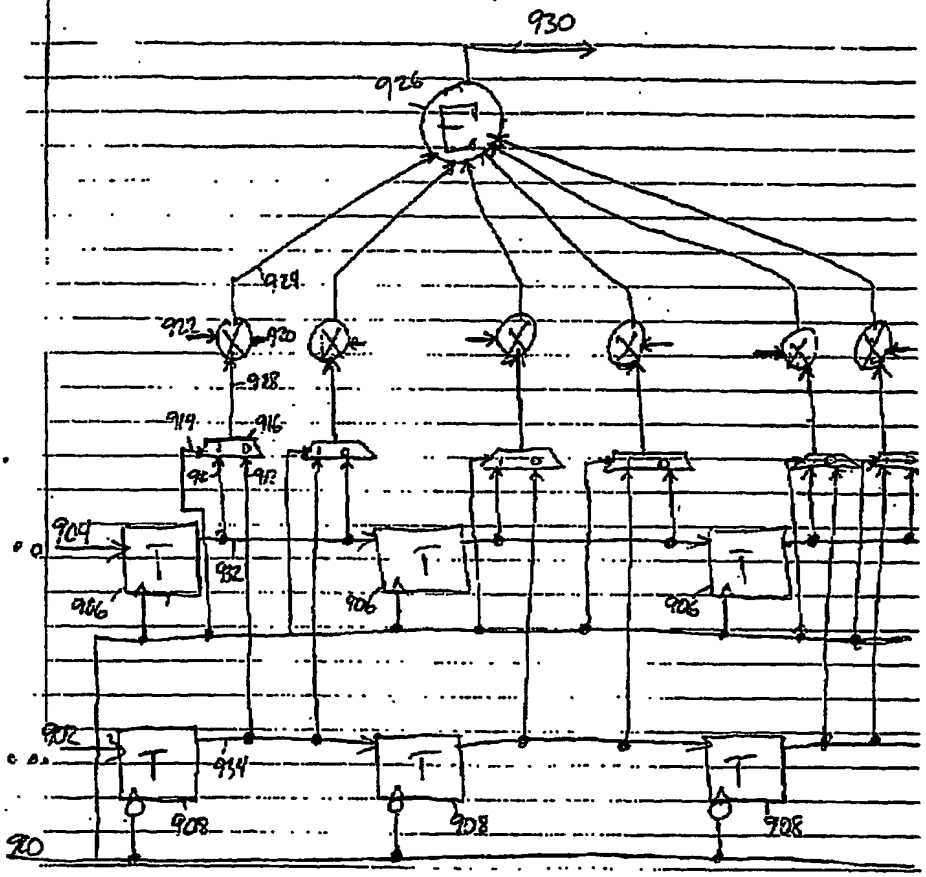
Operating Frequency Reduction For Transversal FIR filter

FIG. 9



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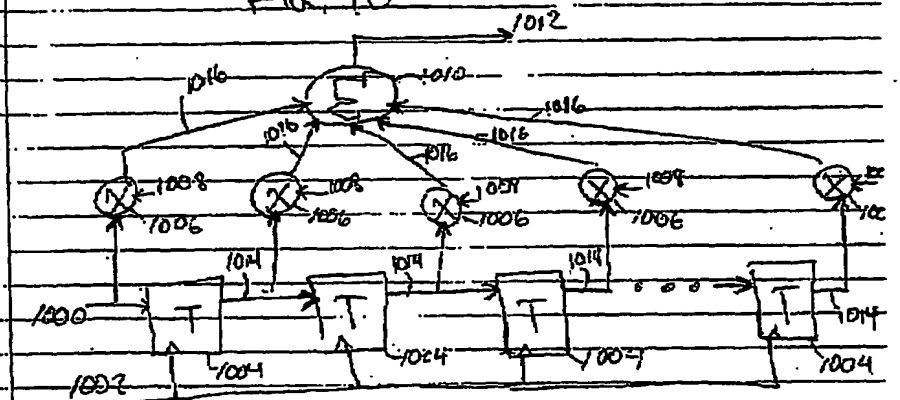
- Operating Frequency Reduction For Transversal FIR Filter

FIG. 10



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Operating Frequency Reduction for Transversal Fiber Filter